DESIGN AND IMPLEMENTATION OF A DSP-BASED THREE-PHASE SHUNT ACTIVE POWER FILTER

Nguyen Khanh Tu Tam¹, Nguyen Van Nho¹, Huynh Huu Tai², Nguyen Le Huy Bang³
¹,²,³ Ho Chi Minh University of Technology

ABSTRACT
The active power filter (APF) has been proved to be an advanced power electronics device, which is used to compensate harmonics and reactive power of non-linear loads. In this paper, the basic operation principle and structure of the three-phase APF are analyzed. The design issues and the implementation of the control algorithm using DSP are also presented in detail. Some experimental results are shown to verify the effectiveness of the APF system.

KEYWORDS: Active power filter, instantaneous reactive power theory, design issues, DSP-based implementation.

1. INTRODUCTION
The harmonic problem and power quality have become serious concerns due to the increasing of nonlinear loads in many power electronic equipments. Conventionally, the passive filters have been used to solve harmonic current problems. However, they bring many disadvantages for the power system like electromagnetic interference, resonance, fixed-compensation etc. Among many compensated methods to cope with these disadvantages, APF is considered to be an effective and practical solution. Its dynamical characteristics overcome the previous drawbacks of the passive filters. When being connected in parallel with a power system, APF acts as a controlled harmonic current source, injecting simultaneously suitable currents into the power system to eliminate the harmonic content caused by nonlinear loads and to obtain a unity input power factor.

This paper analyzes the working principle, design issues and control method implemented on a DSP-controller of the shunt APF. Some experimental results with good performance in both reactive power compensation and harmonic suppression are shown to verify the effectiveness of the shunt APF.

2. STRUCTURE AND WORKING PRINCIPLE

![Figure 1. The structure of Three Phase, Three-Wire Shunt Active Power Filter](image)

The main circuit structure of a three-phase shunt active power filter (SAPF) is shown in Figure 1. \(v_a, v_b,\) and \(v_c\) are the input phase voltages which are Y-connected. A commonly used three-phase rectifier is chosen as a nonlinear load which produces nonlinear load currents \(i_{a}, i_{b}, i_{c}\). The SAPF block is connected in parallel with the power system. When the SAPF is not in
use, the three line currents $i_{sa}, i_{sb}, i_{sc}$ are equal to the three nonlinear load currents. Under operating condition, the SAPF injects compensated currents which are equal in magnitude but opposite in sign with respect to harmonic current components at the point of connection. The harmonic distortion is therefore compensated and balanced sinusoidal source currents are obtained.

3. CONTROL METHOD

In this paper, the control algorithm for reference current signal generation is based on the instantaneous reactive power (p-q) theory. This theory was proposed by Akagi in 1983 [4] and since then has been widely used because of its flexibility and effectiveness in harmonic suppression and dynamic power factor correction.

In p-q theory, the instantaneous values of three-phase load current and three-phase voltage are transformed to $\alpha \beta$ as shown in equation (1) and (2).

$$
\begin{bmatrix}
i_o \\
i_{ia} \\
i_{ib} \\
i_{ic}
\end{bmatrix} = \frac{2}{\sqrt{3}} \begin{bmatrix}
\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\
1 & -1/2 & -1/2 \\
0 & \sqrt{3}/2 & -\sqrt{3}/2
\end{bmatrix}
\begin{bmatrix}
i_a \\
i_b \\
i_c
\end{bmatrix}
$$

$$
\begin{bmatrix}
v_o \\
v_a \\
v_b \\
v_c
\end{bmatrix} = \frac{2}{\sqrt{3}} \begin{bmatrix}
\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\
1 & -1/2 & -1/2 \\
0 & \sqrt{3}/2 & -\sqrt{3}/2
\end{bmatrix}
\begin{bmatrix}
v_a \\
v_b \\
v_c
\end{bmatrix}
$$

The load side instantaneous real, imaginary and zero sequence power components are then calculated as

$$
\begin{bmatrix}
\bar{p} \\
\hat{p} \\
\bar{q}
\end{bmatrix} = \frac{2}{\sqrt{3}}
\begin{bmatrix}
v_o & 0 & 0 \\
v_a & v_\beta & 0 \\
0 & -v_\beta & v_a
\end{bmatrix}
\begin{bmatrix}
i_o \\
i_a \\
i_\beta
\end{bmatrix}
$$

To independently select the portions of powers to be compensated, these powers are separated into their average and oscillating parts as follow:

$$
p = \bar{p} + \hat{p}, \quad q = \bar{q} + \hat{q}, \quad \bar{p}_o = \bar{p}_o + \hat{p}_o \quad (4)
$$

In (4), the average real power $\bar{p}$ is the only desirable component that the power system needs to supply to the load. All other power components described by $\bar{q}, \bar{q}, \bar{q}, \bar{p}_o$ should be compensated by the SAPF. Additionally, to keep the voltage of the dc capacitor constant during the SAPF operation, an extra amount of real power represented by $\bar{p}_{loss}$ should be added to the compensating real power. As a result, the SAPF should be controlled to compensate the real power $\bar{p}_o + \hat{p} - \bar{p}_{loss}$ and the whole imaginary power $\bar{q} + \hat{q}$. The compensating current calculation in $\alpha \beta \alpha$ coordinate is then the derived as:

$$
\begin{bmatrix}
i_{fa} \\
i_{fb} \\
i_{fc}
\end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix}
v_a & -v_\beta \\
v_\beta & v_a \\
0 & -\sqrt{3}/2 & \sqrt{3}/2
\end{bmatrix}
\begin{bmatrix}
\bar{p} - \bar{p}_o + \bar{p}_{loss} \\
-q
\end{bmatrix}
$$

The reference compensating phase currents in $abc$ axis is computed in terms of the compensating currents in $\alpha \beta \alpha$ coordinate:

$$
\begin{bmatrix}
i_{fa} \\
i_{fb} \\
i_{fc}
\end{bmatrix} = \sqrt{2}/3
\begin{bmatrix}
\frac{1}{\sqrt{2}} & 1 & 0 \\
\frac{1}{\sqrt{2}} & -1/2 & \sqrt{3}/2 \\
1/\sqrt{2} & -1/2 & -\sqrt{3}/2
\end{bmatrix}
\begin{bmatrix}
i_{fa} \\
i_{fb} \\
i_{fc}
\end{bmatrix}
$$

Figure 2 shows a block diagram of the reference current generation method using p-q theory developed for three-phase three-wire SAPF. The instantaneous three-phase load currents and three-phase voltages are utilized to calculate the load side real and imaginary powers. The real power is then separated into average power $\bar{p}$ and oscillating power $\hat{p}$ by using an IRR filter with cut-off frequency of 20Hz.

To guarantee the controllability of the SAPF system, the dc voltage regulator is added to the control scheme to keep the dc voltage fixed at a value higher than the peak value of the ac bus voltage. This control block is a simple PI controller which P and I coefficients are determined by using the Ziegler-Nichols tuning method. The input of the PI controller is the dc voltage error and output is the average real power.
The zero sequence power \( p_0 \) is always zero due to the absence of zero sequence current component in three phase, three wire systems. Thus the compensating currents is then calculated in terms of the compensated real power \(-\bar{p} + p_{\text{loss}}\), imaginary power \( \bar{q} \) and \( v_\alpha, v_\beta \).

To simply implement the APF PWM modulation and achieve fast dynamic response control, a hysteresis current controller is used.

Based on the deviation between the reference compensating current and actual current, the hysteresis comparator will generate PWM signals which input to the dead-zone circuit before reaching the SAPF gate driver circuit.

4. DIGITAL CONTROLLER FOR SHUNT ACTIVE POWER FILTER

4.1 Hardware Structure

Figure 4 shows the block diagram of SAPF using a 32 bit floating point DSP TMS320F28335 as a digital controller. The hardware consists three main parts: measurement circuit using Hall current and voltage sensors, DSP-based control circuit and driver circuit. The measurement circuit converts three phase current and voltage signal into 0V~3V level signals which are fed to the A/D module of the control circuit. The main role of the DSP is to calculate the reference compensating current based on the p-q theory and do the PWM modulation of current tracking control using hysteresis current controller.

The output signal generated by the control circuit is driven into the driver circuit. Six isolated dc supply voltages of \( \pm 15V \) level are used in the driver circuit to change the driving signal level from 0V, 3V to -15V,+15V respectively.

4.2 Software implementation

The flowcharts of DSP main routine and subroutines are shown in Figure 5. Firstly, the system operation configuration and variable initialization are started. Output signal of the control circuit is initially driven to 0V level. Afterwards, the program will continuously checks the dc voltage \( v_{dc} \).

If the dc voltage is greater or equal to peak value of the ac line voltage, the program will be allowed to proceed to the second state.

The A/D channels are assigned to analog signals \( v_a, v_b, v_c, v_{dc} \) and \( i_{la}, i_{lb}, i_{lc}, i_{fa}, i_{fb}, i_{fc} \).
The ADC operation is triggered at the beginning of the second state. Then the program will wait until the ADC interrupt signal happens to read ADC conversion results in the buffer registers. These results are used to calculate the reference compensating currents in abc axis. Based on these reference currents, the new PWM pulse will be updated using hysteresis current control.

Table 1. Specifications of the SAPF prototype

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC supply voltage</td>
<td>42Vrms, 50 Hz</td>
</tr>
<tr>
<td>Output reactor of rectifier</td>
<td>1 mH</td>
</tr>
<tr>
<td>Three-phase diode rectifiers parameters</td>
<td>( L_L = 10\text{mH}, R_L = 47\Omega )</td>
</tr>
<tr>
<td>SAPF inductance</td>
<td>5mH</td>
</tr>
<tr>
<td>SAPF dc link capacitor</td>
<td>5600 ( \mu F ), 400V</td>
</tr>
<tr>
<td>Powers switches</td>
<td>G60N100-BNTD</td>
</tr>
<tr>
<td>Regulated dc voltage</td>
<td>150V</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>20khz</td>
</tr>
</tbody>
</table>

Figure 6. Control system of SAPF (measurement circuit, DSP controller and gate driver circuit)

Figure 7 shows experimental waveforms observed in the same scope including the A-phase supply voltage, A-phase load current \( i_{LA} \), compensating current \( i_{fA} \) and compensated supply current \( i_{SA} \). The waveform of \( i_{SA} \) before compensating is equal to the current of non-linear load \( i_{LA} \). This current will be shifted by an angle depending on values of \( R_L, L_L \) with respect to the input voltage. However, as shown in Figure 7, the waveform of \( i_{SA} \) after compensation is nearly sinusoidal and nearly in phase with its respective input phase voltage.

The FFT analysis of \( i_{SA} \) depicted in Figure 8 and 9 indicates that the SAPF can largely

Figure 5. Flowchart of the SAPF control algorithm

The sampling period is set at 50\( \mu \)s by using the CPU timer interrupt. The updated PWM pulse will be generated to the IO port each time the CPU timer interrupt happens.

5. EXPERIMENTAL RESULTS

To demonstrate the effective performance of the SAPF, an experimental prototype which control system shown in Figure 6 is built and tested in the laboratory. The specifications of the prototype are described in Table 1. In the experiment, the three phase bridge rectifier is used to imitate the non-linear load.
improve the THD of the supply current. The THD is reduced from 20% before compensation to 1.2% after compensation.

6. CONCLUSION

This paper has discussed the design and implementation of the shunt active power filter. The digital controller of the system is presented in detail. The experimental results with good performance in harmonic compensation and power factor correction are given to verify the validity and effectiveness of the SAPF in power quality compensation.

7. REFERENCES


Contact information:
Nguyen Khanh Tu Tam
Tel: (+84)917350242
Email: tam_khanh bk@yahoo.com
University of Technology, 268 Ly Thuong Kiet, 14 ward, district 10, Ho Chi Minh city, Viet Nam